IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kevin J. Ryan	Examiner: James Peikari	
Serial No.:	09/434,654	Group Art Unit: 2186	
Filed:	November 5, 1999	Docket: 303.306US4	
Title:	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

This paper is in response to the Office Action mailed on March 14, 2002. Please amend the above-identified patent application as follows.

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the Office action, thereby moving the deadline for response from June 14, 2002 to July 14, 2002.

IN THE DRAWINGS

Enclosed is new Figure 6. New Fig. 6 is believed supported by the original specification. As an example, the specification describes a DRAM at several locations. One of ordinary skill in the art, under 35 U.S.C. §112 would understand these features. No new matter is believed proposed. Entry of the proposed new Figure 6 is respectfully requested.

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning at page 8, line 3 is amended as follows:

Each memory subsystem 130 includes a C/A buffer register 131, a plurality M of memory devices 135 and a data buffer register 141. C/A buffer register 131 receives and latches the command and address information from C/A bus 110. As illustrated in Figure 1, buffer register 131 is connected between the command and address bus 110 and the plurality of memory devices